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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.				
10/826,215	04/16/2004	Brian Hang Wai Yang	RZMI-P306	1173				
32986 IPSG, P.C. P.O. BOX 700640 SAN JOSE, CA 95170	7590 09/18/2007		<table border="1"><tr><td colspan="2">EXAMINER</td></tr><tr><td colspan="2">MAHMOUDZADEH, NIMA</td></tr></table>		EXAMINER		MAHMOUDZADEH, NIMA	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/826,215	YANG ET AL.	
	Examiner	Art Unit	
	Nima Mahmoudzadeh	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04/16/2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--------------------------------------------------------------------------------------|-------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. ____. |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al. (US Patent Publication No. 2003/0009599).

Regarding claim 1, Lee et al. teach a stacked switch using a resilient packet ring protocol comprising:

a plurality of switch modules (Fig. 1, 102A-102D) coupled to one another in a ring topology (Fig. 1) and each having a plurality of external terminals for interfacing with external devices, where each switch module includes:

(a) an external interface (Fig. 1, Ethernet and TDM) for communicating with the external terminals (Fig. 1, Ethernet and TDM), the external interface configured to communicate using a communication protocol (Fig. 1); and

(b) an internal interface (Fig. 2) for communicating with other switches (Fig. 2, 204 and 206), the internal interface using a

resilient packet ring (RPR) protocol (Paragraph [0023], Fig. 1).

Regarding claim 2, Lee et al. teach the stacked switch of claim 1, wherein each switch module further includes:

(c) a controller coupled (Fig. 2, 202) to the external interface and the internal interface and configured to selectively communicate information between the external interface and the internal interface (Fig. 2).

Regarding claim 3, Lee et al. teach the stacked switch of claim 2, further comprising:

a master management processor (Fig. 3, 300) coupled to one or more switch modules (Fig. 2, 200) and configured to provide instructions regarding the communication of information between each switches' external interface and internal interface (Fig. 2, 208 and 210), and to control data flow (Fig. 3, 330 and 342); and
a slave management processor (Fig. 3, 302) coupled to the master management processor (Fig. 2) through at least one switch and one or more switch modules (Fig. 1 and Fig. 2) and configured to provide instructions regarding the communication of information between each switches' external interface and internal interface, and to control data flow (Fig. 1

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and Fig. 2).

Regarding claim 4, Lee et al. teach the stacked switch of claim 3 further comprising:

the master management processor is configured to assign the master/slave relationship based

on predetermined criteria (Paragraphs [0036] and [0037]); and

the slave management processor is configured to become a master management processor if the master management processor fails (Paragraphs [0036] and [0037]).

Regarding claim 5, Lee et al. the stacked switch of claim 3, further comprising:
a link aggregation port coupled to one or more switch modules' external terminals (Fig. 2, 210) and

configured to selectively aggregate information to and from the switch modules (Fig. 1 and Fig. 2).

Regarding claim 6, Lee et al. the stacked switch of claim 5, further comprising:
a memory configured (Fig. 2) to store statistics associated with the communication of data through at
least one module in the switch (Paragraph [0025] and Fig. 2); and
wherein the master processor (Fig. 2) is configured to evaluate the statistics in the

memory and to generate a link signal representative of desired links/ports to be aggregated (Fig. 2); and
wherein the link aggregation port (Fig. 2) is configured to respond to the link signal and to dynamically set one or more switch modules' external terminals to selectively aggregate information to and from the switch modules (Fig. 2).

Regarding claim 7, Lee et al. the stacked switch of claim 6, wherein:
the master processor is configured to introduce marker information into the data to ensure
that the integrity of the data is reasonably maintained (Packet switching utilizes error detection to detect errors. Fig. 2), when a link aggregation is modified.

Regarding claim 8, Lee et al. a method of switching data through a stacked switch using a resilient packet ring protocol,
the stacked switch having a plurality of modules, where each module includes external interface for communicating with external terminals and an internal interface for communicating with other switches using a resilient packet ring (RPR) protocol, comprising the steps of:
storing statistics associated with the communication of data through at least one module in the switch (Fig. 2 and Fig. 3 and Paragraph [0025]); and
evaluating the statistics in the memory (Fig. 2, 214 and 222) and to generate a link signal representative of desired links/ports to be aggregated (Fig. 2, 204 and 206

and Paragraph [0025]); and

selectively activating a link aggregation port (Fig. 3, 326, 336, 332, and 338) to respond to the link signal and to dynamically set one or more switch modules' external terminals (Fig. 2, 210 and 208) to selectively aggregate information to and from the switch modules (Fig. 2, 214).

Regarding claim 9, Lee et al. the method of claim 8, further comprising the step of:

Selectively introducing marker information into the data (Packet switching utilizes error detection to detect errors. Fig. 2) to ensure that the integrity of the data is reasonably maintained when a link aggregation is modified (Fig. 2, 214).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Mor (US Patent No. 7,054,264) teaches interconnect and gateway protection in bidirectional ring networks

Mor et al. (US Patent Publication No. 2002/0186667) teach communication in a bidirectional ring network with single-direction receiving

Oz et al. (US Patent No. 7,110,355) teach automatic side selection in double-ring topologies

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4. Any responses to this Office Action should be **faxed** to (571) 273-8300 or **mailed** to:

Commissioner for Patent
P.O. Box 1450
Alexandria, VA 22313-1450

Hand-delivered responses should be brought to
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nima Mahmoudzadeh whose telephone number is (571) 270-3527. The examiner can normally be reached on Monday - Friday 7:30am - 5:00 pm EST.

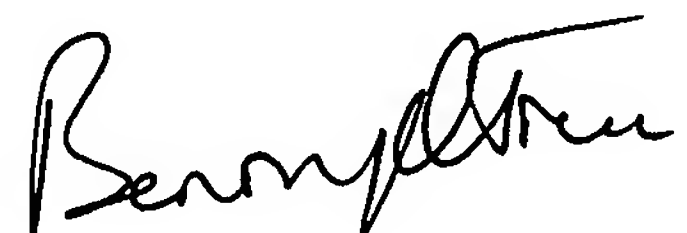
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benny Q. Tieu can be reached on (571) 272-7490. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nima Mahmoudzadeh

AU 2609


BENNY Q. TIEU
SPE/TRAINER